

The Future of Sealing Technology

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This is the final article in a three-part series on high-technology sealing components used to create and safeguard ultraclean manufacturing environments

Introduction

The future—truly—is here today. The semiconductor industry is preparing to make the 22 nm technology node production ready. And the transition to the next-generation 450 mm wafer size is a hot topic of discussion. The days of denial and skepticism about these technological leaps are over. Now they are only a matter of time and economics.

The semiconductor industry has “broken the rules” many times over. This includes pushing the envelope with the Periodic Table of Elements on many fronts. There is no longer a myopic focus on silicon-based technology and growing oxide layers. For example, technologists today are overcoming copper’s electromigration issues, which once made it an unusable metal in microelectronics processing. New precursors such as hafnium are expanding the range of elements that can be used in semiconductor processing (Figure 1) while, at the same time, cleaning-gas technology is progressing from today’s aggressive NF_3 cleans to even harsher F_2 cleans. Immersion lithography and extreme ultraviolet (EUV) imaging have changed the way circuit patterns are printed onto wafers. The advent of 3D device architecture is creating new realities in semiconductor manufacturing. While all of these technological advances continue to drive miniaturization, they also shrink tolerances for particulate contaminants that can cause “killer defects” and endanger the manufacturability of advanced ICs.

Today’s Critical Sealing Applications

To meet semiconductor-grade sealing requirements for particle sizes and cleanliness specifications, sealing experts have developed a class of materials called perfluoroelastomers or FFKM¹ (Figure 2). Sealing elements made from perfluoroelastomers such as Perfrez^{®2} exhibit excellent chemical resistance and incorporate

tetrafluoroethylene (TFE) backbones that ensure the integrity of ultraclean environments. As I discussed in my previous article, these seals demand sensitive care and handling so it is an absolute necessity that anyone installing, replacing or storing perfluoroelas-

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tomers understand how to use them properly for the best results.

As fully fluorinated monomers, perfluoroelastomers have one of the strongest chemical structures—unbreakable due to the bond between the carbon and fluorine atoms. These polymers have no available hydrogen positions, which differentiates them from FKM elastomers (Figure 3). The hydrogen positions make those elastomers susceptible to chemical attack, and may ultimately break down even under the weakest of chemicals. They have virtually no chance of withstanding exposure to the harsh oxygen and fluorine environments that are typical in semiconductor processing.

Along with the base polymer, cure-site monomers give perfluoroelastomers their elasticity. These monomers must be matched to the filler systems, giving these elastomers their physical properties. It should be understood that there are variations of these monomers that can affect their use. For example, TAIC (Triallyl Isocyanurate) provides the best overall chemical resistance and a short curing cycle, which is advantageous for lead-time value, but it has a limited temperature range that cannot exceed 230°C. Triazine is a great high-temperature cure-site

monomer that can be used in temperatures up to 310°C, but triazine cannot endure harsh chemistries, presents sticking issues and requires a long curing cycle. Bisphenol can handle harsh chemicals and high temperature ranges, but it has some limiting physical properties such as high compression. In the complex process of selecting the right seal, it is imperative to understand these differences to prevent costly misapplications.

The most critical area in sealing today may be slit valves, which are also referred to as slot valves or gate valves. In these highly sensitive areas within semiconductor manufacturing equipment, in-process wafers squeeze through the valves' tight openings, making particle generation an immediate threat. To avoid potential contamination caused by wafers coming into contact with slit valves, bonded gates were created (Figure 4). Particle generation is greatly reduced with bonded gates because there is no compression set or movement of the seals in their housings. In addition, the profile of the gate itself and the way in which the sealing element is installed reduces the chance of metal-to-metal contact. However, issues such as mechanical misalignment and the seal's susceptibility to harsh chemistries must still be watched carefully.

Designing Tomorrow's Sealing Solutions

Only a few years ago, it was unimaginable that particles smaller than a micron would present any problems. Now particles measured in mere nanometers can cause yield-reducing defects. Yet surprisingly, selecting sealing elements for a specific application is too often done without considering all of the conditions that the seal will encounter or the composition of the seal itself. For instance, with many current sealing products made with fillers measuring 40 microns to 70 microns in size,

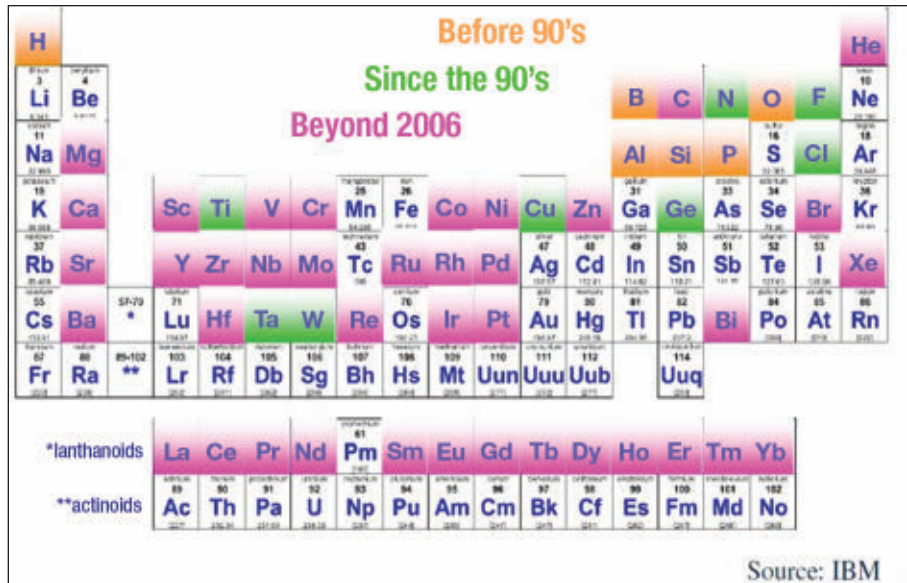


Figure 1. Elements employed in semiconductor processing: before the 1990s; since the 1990s; beyond 2006

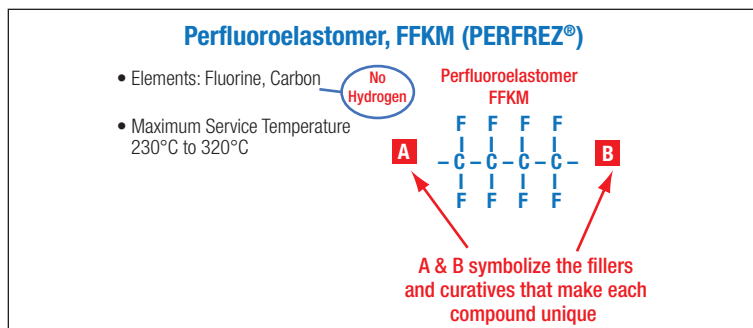


Figure 2. Characteristics of perfluoroelastomers

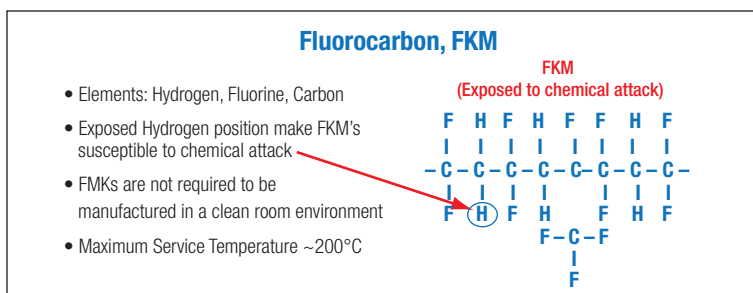


Figure 3. FKM elastomer showing exposed hydrogen position

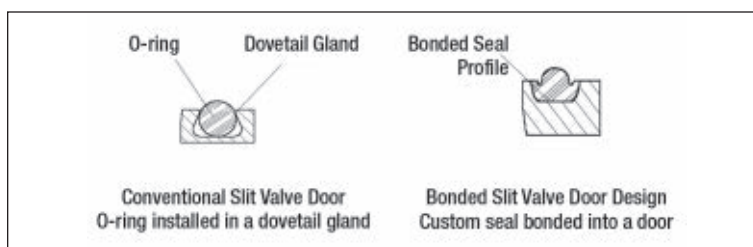


Figure 4. Conventional and bonded slit valve doors

it's clear that today's seals must be not only efficient barriers against nanoparticles, but must also have the design and composition to avoid becoming contamination dangers themselves.

To help ensure that seals do not contribute particles when installed, it is imperative that they be manufactured in cleanrooms following ultrapurity practices and process controls similar to those used in semicon-

ductor fabrication. The objective is to eliminate any metals and contaminants from seal manufacturing. In production areas, seal manufacturers should operate under Class 1,000 environmental conditions. Then when the finished seals are cleaned and packaged for shipment to customers, Class 100 conditions will help O-rings and other products to maintain their integrity all the way to the point of use.

Quantifying seal performance in various applications is a critical industry need. Pioneering tomorrow's sealing solutions is a key objective at SEMATECH's EUV Mask Blank Development Center in Albany, N.Y. The availability of defect-free masks is cur-

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SEMATECH has established a unique facility to support the metrology, characterization and evaluation of EUV mask blank defects and the characterization of particles as small as tens of nanometers. The progress in developing sealant materials and technology will benefit immensely the reduction of EUV mask blank defects and promote the commercialization of EUV lithography beyond the 22 nm HP node down to 6nm. The sealant solutions for current technology applications should be able to resist harsh conditions such as plasma and show no degradation during mechanical cycling with minimal outgassing and no particle generation down to a size of 40 nm.

Making Better Seals

New semiconductor-processing capabilities—from 22 nm linewidths to 3D device structures—bring with them requirements for greater cleanliness. This puts pressure on seal designers to advance the state of the art in sealing solutions. In producing tomorrow's generation of O-rings and other seals, seal manufacturers must begin to implement higher levels of purity and quality control than they have ever used before. Developing standards for things such as low-defect sealing materials and common means to measure them—as the F51 SEMI Standards Task Force began recently—is needed for the collective good of the global semiconductor industry. It is imperative that integrated device manufacturers (IDMs), foundries, equipment suppliers, seal manufacturers and industry consortia such as SEMATECH work together to ensure that sealing solutions continue to evolve and keep pace with advances in semiconductor production.

rently the most critical technology gap hindering the commercialization of extreme ultra-violet (EUV) lithography.

The current industry requirement specifies that EUV blanks contain 0 defects >150 nm, considered to be killer defects, and ≤ 0.13 defect/cm² defect density above 50 nm. SEMATECH is producing EUV blanks with 0.1 defect/cm² defect density above 70 nm at a yield of 70% as a result of current progress. This semiconductor research consortium considers the defects originated by seals in the deposition system of EUV blanks to be one of the prominent sources of defects.

The sealing industry needs to find ways to develop the next generation of materials, polymers and fillers that will fit with both new process technologies and the hardware requirements of the future. Pivotal challenges include reducing the size of the fillers that are mixed with the polymers, improving the cleanliness of the polymers themselves, and establishing a collaborative industry effort to assess which seal-making materials and formulations yield the best results. The stakes are high because of the key role that seals play in enabling the nanoelectronic devices of the future. G&I

1. Fluorocarbons (FKMs) and perfluoroelastomers (FFKMs) are the two most notable materials used in making sealing components. Among the notable differences, FKMs are comprised of hydrogen, fluorine and carbon atoms, whereas FFKMs contain only fluorine and carbon atoms. The absence of hydrogen atoms gives FFKMs greater chemical and thermal resistance, making this material more impervious to the harsh environments used in the semiconductor industry.
2. Perfrez is a registered trademark of Applied Seals Co., Ltd.

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